REMARKS

This application has been reviewed in light of the Office Action dated February 10, 2003. Claims 1, 2, 4, 5, 7-19, 21, 22, 24-38, and 49-54 are pending in this application, with Claims 1, 18, 49, and 52-54 in independent form. Claims 52-54 have been added to provide Applicants with a more complete scope of protection. Claims 1, 18, and 49-51 have been amended to define more clearly what Applicants regard as their invention. Favorable reconsideration is requested.

As an initial matter, Applicants respectfully request that the PTO-1449 form for the Information Disclosure Statement filed on November 28, 2001 be initialed and returned, indicating that the cited references have been considered. A copy of that Information Disclosure Statement, along with a copy of the stamped postcard indicating receipt by the U.S. Patent and Trademark Office, are attached herewith.

Claims 1, 2, 4, 5, 7-12, 15, 16, 18, 19, 21, 24-29, 32, 33, 35, 38, and 49-51 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis (U.S. Patent No. 5, 589,847) in view of Yamaguchi (U.S. Patent No. 5,438,342) and Shinya (U.S. Patent No. 5,170,158), and Claims 13, 14, 17, 30, 31 34, 36, and 37 were rejected under Section 103(a) as being unpatentable over Lewis in view of Yamaguchi and Shinya, and further in view of Misawa et al. (U.S. Patent No. 5,250,931).

Applicants submit that amended independent Claims 1, 18, and 49 and newly added independent Claims 52-54, together with the remaining dependent claims, are patentably distinct from the proposed combination of the cited prior art for at least the following reasons.

Claim 1 requires a driving apparatus including a matrix substrate, an input terminal, a vertical scanning circuit, a sequencing circuit, a horizontal scanning circuit, a latch circuit, a D/A converter, plural signal transfer switches, a selection circuit, polarity inversion circuitry, and a buffer. The matrix substrate has plural pairs of switching elements and picture elements provided in a matrix corresponding to intersecting points of scanning lines and signal lines. The input terminal is for receiving a sequence of digital video data in a serial fashion. The vertical scanning circuit is for outputting a scanning signal to the scanning lines. The sequencing circuit is for changing an initial sequencing order of the digital video data received at the input terminal into a different sequencing order, and for serially outputting the digital video data in the different sequencing order. The horizontal scanning circuit is for controlling a sampling of the digital video data in the different sequencing order. The latch circuit is for memorizing the digital video data in its different sequencing order in synchronism with an output from the horizontal scanning circuit. The D/A converter is for converting an output from the latch circuit into analog signals. The plural signal transfer switches are provided between the D/A converter and the signal lines. The selection circuit is for selecting at least one of the signal transfer switches so as to output the analog signals to the matrix substrate in the same order as the different sequencing order of the digital video data. The polarity inversion circuitry controls the D/A converter to alternately invert the analog signal from the D/A converter. The buffer is disposed between the D/A converter and the selection circuit, which stores the analog signal from the D/A converter, and outputs the stored signal to the plural signal transfer switches. Also, a number M of the D/A converters is less than a number N of the switching elements arranged in a horizontal direction, and analog signals are sequentially

inputted from particular ones of the M D/A converters to N/M plural switching elements arranged in a horizontal direction, via a number M of the buffers.

Some of the benefits of this invention include a reduction of size of external driving circuits and a reduction of power consumption. (See page 17, line 24, to page 18, line 22 of the specification.)

One important feature of Claim 1 is the sequencing circuit for changing an initial sequencing order of the digital video data serially received at an input terminal into a different sequencing order, and for serially outputting the digital video data in the different sequencing order. Support for this feature can be found in the specification at least at page 15, lines 16-27, which is described in reference to Figures 1, 2A, and 2B. This portion of the specification describes that this embodiment has 1/4 as many D/A converters 12, 13 as there are picture elements 19 in the horizontal direction. The outputs of the D/A converters 12, 13 are fed to respective picture elements 19 through buffers 14, 15 by turning on and off the groups of four switches 17 under the control of outputs S1 - S4 of the transfer switch selection circuit 16. Because each output of the D/A converters 12, 13 is fed to a group of four picture elements 19 via the switch circuit 16 and switches 17, the picture signals should be introduced for every fourth picture element. Therefore, the circuit includes a sequencing means 1 for sequencing an input picture signal data such that it outputs a data signal for every fourth picture element. Figure 2A shows an input signal of 1, 2, 3, 4, . . . 16 and Figure 2B shows the changed-sequence output signal of 1, 5, 9, 13, . . . 16. (It is to be understood, of course, that the scope of Claim 1 is not limited to the details of this embodiment, which is referred to only for purposes of illustration.)

As a disclosure of the sequence changing circuit just discussed, the Office Action points to the shift register 505 shown in Figure 15A of Lewis. (See pages 2-3 of the Office Action.) However, Lewis describes the shift register 505 as serially loading input data, and then outputting the data in parallel to a set of digital latches 515a-c. (See column 10, lines 28-30.) Therefore, Applicants understand that the shift register 505 is a serial-parallel shift register, the operation of which takes a string of data as input, one bit at a time, and then outputs, in parallel, the string of data in the same sequence it was input. (See Jefferson C. Boyce, Digital Logic Operation and Analysis 323, 325 (1982). Copies of the cited pages are attached to this Amendment). For example, if the data 1101 is serially read into a serial-parallel shift register, the parallel output of the shift register would also be 1101. Therefore, Applicants submit that a serial-parallel shift register does not change a sequencing order of input data in the manner required by Claim 1.

To further distinguish the sequence changing circuit of Claim 1 from the serial-parallel shift register 505 of Lewis, Applicants have amended Claim 1 to require that the sequencing circuit for changing an initial sequencing order of the digital video data *serially* outputs the digital video data in the different sequencing order. In contrast, the serial-parallel shift register 505 of Lewis outputs in parallel.

For at least these reasons, Applicants submit that Lewis would not teach or suggest to a person having ordinary skill in the relevant art the circuit for changing an initial sequencing order of the digital video data serially received at an input terminal into a different sequencing order, and for serially outputting the digital video data in the different sequencing order, as recited in Claim 1.

Yamaguchi and Shinya appear to be silent with regard to a circuit for changing in initial sequencing order of digital video data. Accordingly, Applicants submit that, at least for the reasons discussed above, the proposed combination of Lewis, Yamaguchi, and Shinya, assuming such combination would even be permissible, would fail to teach or suggest the circuit for changing an initial sequencing order of the digital video data serially received at an input terminal into a different sequencing order, and for serially outputting the digital video data in the different sequencing order, as recited in Claim 1. Applicants submit that Claim 1 is patentable over this prior art, taken separately or in any proper combination.

Independent Claims 18, 49, and 52-54 include a feature very similar to that discussed above in connection with Claim 1 and are believed to be patentable for at least the same reasons.

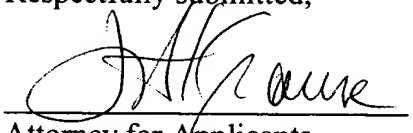
A review of the other art of record has failed to reveal anything that, in Applicants' opinion, would remedy the deficiencies of the art discussed above, as applied against the independent claims herein. Therefore, those claims are respectfully submitted to be patentable over the art of record.

The other rejected claims in this application depend from one or another of the independent claims discussed above and, therefore, are submitted to be patentable for at least the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, individual reconsideration of the patentability of each claim on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicants respectfully request favorable reconsideration and the allowance of the present application.

Applicants' undersigned attorney may be reached in our New York Office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address listed below.

Respectfully submitted,



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